AMENDMENTS TO THE SPECIFICATION

Please amend the paragraph on page 1, line 10, to line 15, as follows:

Conventional technologies relating to a PLL circuit are disclosed in JP-A-9-153797 (especially in Figs. 1 and 4) and Howard M. Berlin, Keiichi Miyata and Fumi Tokuhushi, "PLL no Sekkei to Jitsuyou Kairo (Design of PLL and Practical circuits)", SeaStar, April 1, 1992, especially ~~Especially~~ in Pgs. 1-3, 19-31, 49-50, 59-70 and 91.

Please amend the paragraph on page 2, line 9, to line 23, as follows:

In this kind of PLL circuit, the oscillation frequency f0 of the VCO is divided by the frequency-divider and becomes the reference signal of the frequency fr. The reference signal of the frequency fr is returned to the phase comparator, and is compared with the frequency fi of the index signal by the phase comparator. Then, an error voltage is output. The error voltage is an average direct current voltage in proportion to the frequency difference (fi-fr) and the phase difference $\Delta\varphi$ of the index signal and reference signal. An influence of high-frequency noise is eliminated from the error voltage by the loop filter, and the result is returned to the VCO. Thus, the frequency fo of the VCO varies so as to obtain lower frequency differences (fi-fr), and the loop enters ~~to~~ a capture range state.

Please amend the paragraph on page 3, line 15, to page 4, line 8, as follows:

As disclosed in "Design of PLL circuit and Practical circuit (pgs. 1 to 3), an entire range in which the loop system follows the change in frequency fi of the index signal is called a lock range. The lock range is wider than a frequency range (that is, capture range) in which the loops are in the phase-locked state. The dynamic characteristic of the PLL is basically controlled by the loop filter. When the frequency difference (fi-fr) of the index signal and reference signal is significantly large, the signal cannot pass through the loop filter due to the excessively high frequency. As a result, the signal is determined as being beyond the capture range of the loop, and the lock state is turned off. Once the loops enter ~~to~~ the phase-locked state, the loop speed in accordance with the change in frequency fi of the index signal is only controlled by the loop filter. Additionally, even when the

system is unlocked due to instance noise, the original signal can be captured since the loop filter has a short time memory ability.

Please amend the paragraph on page 4, line 9, to line 15, as follows:

However, as the unlocked time increases, the possibility to adversely affect ~~on~~ the loaded circuits connected to the output terminal of the VCO increases. In order to prevent this, a PLL circuit has been proposed which includes an unlock detecting circuit for detecting a phase unlock of the PLL circuit to turn on/off a PLL operation signal based on the detection signal.

Please amend the paragraph on page 4, line 16, to line 21, as follows:

When the frequency fi of the index signal is changed rapidly and significantly, the phase difference $\Delta\varphi$ increases. Therefore, the oscillation frequency fo of the VCO changes great ~~largely~~. Then, the stable time until the frequency fr of the reference signal agrees with the frequency fi of the index signal increases.

Please amend the paragraph on page 6, line 15, to page 7, line 3, as follows:

In order to solve the problems, according to the invention, in the PLL circuits, there is provided a phase locked loop circuit including a phase comparator for comparing phases of an index signal and reference signal and outputting a signal in accordance with the phase difference, a loop filter for smoothing the output signal of the phase comparator, a controlled oscillator (for example, the VCO ~~VOC~~ and a current controlled oscillator for oscillating at a frequency in accordance with the output signal of the loop filter), and a limiter provided on a path from the output side of the phase comparator to the input side of controlled oscillator for limiting the level of a signal on the path in a predetermined range of phase differences and setting a large gain.

Please amend the paragraph on page 13, line 5, to line 22, as follows:

The limiter 30 has an input resistance 31 having a resistance value R31, which is connected to the output side of the phase comparator 10. The input resistance 31 is connected to a positive

phase input terminal of an operational amplifier 32. A negative phase input terminal of the operational amplifier 32 is connected to the ground GND. The positive phase input terminal of the operational amplifier 32 is connected to an output terminal of the operational amplifier 32 through a feedback resistance 33 having a resistance value R33. Then, the output voltage S30 is output from the output terminal. In accordance with the selection of the resistance values R31 and R33, the gain G (=S30/S10=R33/R31) of the operational amplifier 32 is set to be large ~~largely~~. A forward Zener diode 34 and a reverse Zener diode 35 are connected to the feedback resistance 33 in parallel, and the maximum level and minimum level of the output voltage S30 are limited.

Please amend the paragraph on page 30, line 16, to line 22, as follows:

Like the first embodiment, when a PLL operation is turned on, the limiter 30 operates. Because of the limiter 30, the conversion gain K11 can be set to be large ~~largely~~. Therefore, the jitter characteristic of the output signal SO can be improved. However, as shown in Fig. 7, the response characteristic becomes lower to signals beyond the range determined by the input phase difference $\Delta\varphi$.

Please amend the paragraph on page 35, line 20, to line 23, as follows:

(6) The type, analog or digital, of the loop filter 40 and limiter 30 may depend on the type, analog or digital, of the phase comparator 10 and controlled oscillator. In either case, the invention is applicable.

Please amend the paragraph on page 36, line 16, to line 22, as follows:

When a limiter and a lead-in start signal generating circuit are provided, the output of the limiter is suppressed in a predetermined range of input phase differences. Therefore, signals beyond the range are not responded to. As a result, the above effects can be obtained while minimizing the adverse effects due to the existence of the limiter.